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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,451	09/27/2001	Axel Hertwig	PHDE 000167	5357

24737 7590 10/11/2005

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
GUILL, RUSSELL L	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 10/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,451	HERTWIG ET AL.	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to an Amendment filed July 21, 2005. Claims 1, 6 - 8, and 11 - 12 were amended. No claims were canceled. Claims 1 - 12 have been examined. Claims 1 - 12 have been rejected.

Response to Arguments

2. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection. An updated search yielded new art.

Claim Objections

3. Claim 10 is objected to because of the following informalities: The phrase "a re" appears to be a typographical error of the word, "are". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

a. **Claims 1, 11 and 12** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i. The claim recites, "a first shadow register unit which is connected to the first processor so as to transmit data". It appears to be unclear whether the connection between the first processor and the first shadow register transmits data bidirectionally between the processor and register, or only transmits data from the register to the processor. For the purpose of claim examination, the phrase is interpreted as "a first shadow register

unit which is connected to the first processor so as to transmit data from the first shadow register unit to the first processor". Correction or amendment is required.

ii. The claim recites, "a second shadow register unit which is connected to the second processor so as to transmit data". It appears to be unclear whether the connection between the second processor and the second shadow register transmits data bidirectionally between the processor and register, or only transmits data from the register to the processor. For the purpose of claim examination, the phrase is interpreted as "a second shadow register unit which is connected to the second processor so as to transmit data from the second shadow register unit to the second processor". Correction or amendment is required.

iii. The claim recites, "a multiplexer unit which is connected to the first shadow register unit and the at least one second shadow register unit so as to transmit data". It appears to be unclear whether the connection between the multiplexer and the first and second shadow register units transmits data bidirectionally between the multiplexer and registers, or only transmits data from the multiplexer to the registers. For the purpose of claim examination, the phrase is interpreted as "a multiplexer unit which is connected to the first shadow register unit and the at least one second shadow register unit so as to transmit data from the multiplexer to the first shadow register unit and the at least one second shadow register unit". Correction or amendment is required.

b. **Claims 1, 11 and 12** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative

relationships are: The claim recites, "a register unit, the construction of the first shadow register unit . . . ". The recited register unit appears to be a standalone element which is not attached to any other element. Correction or amendment is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1 and 4 - 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani (U.S. Patent No. 6,314,499) in view of Chrysanthakapoulos (U.S. Patent No. 6,704,819).

a. **Regarding claim 1**:

b. Kermani appears to teach:

i. A multiprocessor array (**figure 2, elements 100, 104, 106, 108; and Abstract**) which includes

ii. a) a first processor shadow register unit (1) which operates within a first clock domain (**figure 2, element 100; it would have been obvious that the element contained a register**) and includes

iii. i) a first processor (**figure 2, element 100; and Abstract; it would have been obvious that the element contained a processor**) (2), and

iv. ii) a first shadow register unit (3) which is connected to the first processor (2) so as to transmit data (**figure 2, element 100; it would have**

been obvious that the element contained a register connected to a processor so as to transmit data),

v. b) at least one second processor shadow register unit (9) (**figure 2, element 104; and Abstract; it would have been obvious that the element contained a register**) which

vi. i) operates within a corresponding second clock domain (**figure 2, element 104; it would have been obvious that the element contained a second clock domain since a clock signal is transmitted**),

vii. ii) includes a second processor (**figure 2, element 104; it would have been obvious that the element contained a processor**) (10), and

viii. iii) a second shadow register unit (11) which is connected to the second processor (10) so as to transmit data (**figure 2, element 100; it would have been obvious that the element contained a register connected to a processor so as to transmit data**), and

ix. c) a synchronous memory unit (**figure 2, elements 102a and 200a**) (17)

x. i) a multiplexer unit (18) which is connected to the first shadow register unit (3) and the at least one second shadow register unit (11) so as to transmit data (**figure 2, element 200a; and column 4, lines 4 - 16**) ,

xi. ii) a register unit (20), the construction of the first shadow register unit (3) and the at least one second shadow register unit (11) and the register unit (20) being identical in respect of function (**figure 2, elements 200a and 100; it would have been obvious that the synchronous memory and the agent 1 both contained a register unit being identical in function**), and

xii. iii) a priority unit (19) for allocating the multiplexer unit (**figure 2, element 102a**) (18) for data transmission to the first shadow register unit (3) or to the at least one second shadow register unit (11) based on at least

one criterion (**figure 2, elements 102a and 190; it would have been obvious that a priority encoder uses a criterion**), the priority unit (19) being connected to the first shadow register unit (3) and to the at least one second shadow register unit (11) via a corresponding asynchronous request line (**figure 2, elements "MEM. ACCESS REQ. 1" and "MEM. ACCESS REQ. 2"; it would have been obvious that the lines were asynchronous since no clock is connected to the arbiter**), said request informing the priority unit of changes in a corresponding shadow register (**column 4, lines 23 – 48**).

c. Kermani does not explicitly teach:

i. a peripheral unit (17) which operates within a peripheral clock domain

d. Chrysanthakapoulos appears to teach:

i. a peripheral unit (17) which operates within a peripheral clock domain (**figure 2, peripheral element 204 connected to computer elements 201 and 206**)

e. The art of Kermani and the art of Chrysanthakapoulos are analogous art because they are both directed to the art of arbitrating access to a shared resource (**Kermani, Abstract**) and (**Chrysanthakapoulos, column 1, lines 5 – 37; and Abstract**).

f. The motivation to use the art of Chrysanthakapoulos with the art of Kermani would have been the benefit recited in Chrysanthakapoulos that the invention provides a technique for device arbitration that does not require any modifications to, nor participation by, the controlled device.

g. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Chrysanthakapoulos with the art of Kermani to produce the claimed invention.

h. **Regarding claim 4**:

i. Kermani appears to teach:

i. A multiprocessor array as claimed in claim 1, characterized in that in order to read out data from the first shadow register unit (3) and/or the at least one second shadow register unit (11) the multiplexer unit (18) is connected thereto in the read out direction (**figure 2, element labeled "CLOCKS, ADDRESS, DATA, CONTROL 1" with bidirectional arrowheads, that connects element 200a and element 100**).

j. **Regarding claim 5**:

k. Kermani appears to teach:

i. A multiprocessor array as claimed in one claim 1, characterized in that requests for access from the first shadow register unit (3) and/or the at least one second shadow register unit (11) to the priority unit (19) are encoded as a one-bit signal (**figure 2, element labeld "MEM. ACCESS REQ. 1" that connects elements 100 and 102a**).

l. **Regarding claim 6**:

m. Kermani appears to teach:

i. A multiprocessor array as claimed in claim 1, wherein said at least one criterion is in conformity with the principle: first-come, first-served (**column 6, lines 3 - 5**).

7. **Claims 2 - 3 and 9 - 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani (U.S. Patent No. 6,314,499) in view of Chrysanthakapoulos (U.S. Patent No. 6,704,819) as applied to claims **1 and 4 - 6** above, and further in view of Mano

(Mano, Morris M.; "Computer System Architecture", second edition, 1982, Prentice-Hall Inc.).

a. Kermani as modified by Chrysanthakapoulos teaches the multiprocessor array, as recited in claim 1 above.

b. **Regarding claim 2**:

c. Kermani does not specifically teach:

i. A multiprocessor array as claimed in claim 1, characterized in that the first shadow register unit (3), the at least one second shadow register unit (11) and the register unit (20) include status flags as well as control/data registers.

d. Mano appears to teach:

i. status flags as well as control/data registers (**page 425, figure 11-12, status register and control register and transmitter register**).

e. The art of Mano and the art of Kermani are analogous art because they both include the problem of asynchronous communications (**Kermani, figure 2**) and (**Mano, page 425, figure 11-12**).

f. The motivation to use the art of Mano with the art of Kermani and Chrysanthakapoulos would have been the benefit of having an integrated circuit available to perform the asynchronous communications (**Mano, page 424, fourth paragraph that starts with "A Teletype has a keyboard . . ."**).

g. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

h. **Regarding claim 3**:

i. Kermani does not specifically teach:

i. A multiprocessor array as claimed in claim 1, characterized in that the first clock domain and/or the at least one second clock domain include more than one processor.

j. Mano appears to teach:

i. A clock domain with more than one processor (**page 458, figure 11-34**).

k. The art of Kermani and the art of Mano are analogous art because they both contain the same problem area of digital logic components used to construct digital equipment.

l. The motivation to use the art of Mano with the art of Kermani would have been the benefit of improved system performance (**Mano, page 454, paragraph four that starts with "The benefit . . ."**). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

m. **Regarding claim 9**:

n. Kermani does not specifically teach:

i. A multiprocessor array as claimed in claim 1, characterized in that the peripheral unit (17) is constructed as an infrared interface, UART interface or USB interface.

o. Mano appears to teach:

i. A UART interface (**Mano, page 424, fourth paragraph that starts with "A Teletype has a keyboard . . .", last sentence**).

p. The motivation to use the art of Mano with the art of Kermani and Chrysanthakapoulos would have been the benefit of having an integrated circuit

available to perform the asynchronous communications (**Mano, page 424, fourth paragraph that starts with "A Teletype has a keyboard . . ."**).

q. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

r. **Regarding claim 10**:

s. Kermani does not specifically teach:

i. A multiprocessor array as claimed in claim 1, characterized in that the first shadow register unit (3) and/or the at least one second shadow register unit (11) are connected to the associated processor (2, 10) via an interrupt (8, 16).

t. Mano appears to teach:

i. a register unit (11) is connected to an associated processor (2, 10) via an interrupt (**page 157, figure 5-8 and last paragraph; and page 159, first and second paragraphs**) (8, 16).

u. The motivation to use the art of Mano with the art of Kermani and Chrysanthakapoulos would have been the benefit of allowing the processor to keep busy with other tasks (while waiting for data transfer) (**Mano, page 157, last paragraph**).

v. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

w. **Regarding claim 11**:

x. Most all of claim 11 is taught as in claim 1 above. The differences are taught below.

y. Kermani does not specifically teach:

i. A communications terminal using a multiprocessor array.

z. Mano appears to teach:

i. A communications terminal (**page 156, section 5-5 Input-Output and Interrupt, first and second paragraph**).

aa. The motivation to use the art of Mano with the art of Kermani and Chrysanthakapoulos would have been the benefit of allowing the processor to serve a useful purpose by communicating with the external environment (**Mano, page 156, section 5-5 Input-Output and Interrupt, first paragraph**).

bb. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

cc. **Regarding claim 12**:

dd. Most all of claim 12 is taught as in claim 1 above. The differences are taught below.

ee. Kermani does not specifically teach:

i. A portable device using a multiprocessor array.

ff. Mano appears to teach:

i. A portable device (**page 156, section 5-5 Input-Output and Interrupt, first and second paragraph, especially the teletypewriter; it would have been obvious that a teletypewriter was a portable device since it is able to be delivered as a unit without being assembled from pieces on location**).

gg. The motivation to use the art of Mano with the art of Kermani and Chrysanthakapoulos would have been the benefit of allowing the processor to

serve a useful purpose by communicating with the external environment (**Mano, page 156, section 5-5 Input-Output and Interrupt, first paragraph**).

hh. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Mano with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

8. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani (U.S. Patent No. 6,314,499) in view of Chrysanthakapoulos (U.S. Patent No. 6,704,819) as applied to claims **1 and 4 - 6** above, and further in view of Levenstein (U.S. Patent No. 5,586,331).

a. Kermani as modified by Chrysanthakapoulos teaches the multiprocessor array, as recited in claim **1** above.

b. **Regarding claim 7**:

c. Kermani does not specifically teach:

i. A multiprocessor array as claimed in claim 1, wherein said at least one criterion in conformity with the principle: all shadow register units (3, 11) are served successively.

d. Levenstein appears to teach:

i. Resource arbitration is served successively (**column 8, lines 35 - 42**).

e. The art of Levenstein and the art of Kermani are analogous art because they are both directed to the art of multiple processing agents connected to shared memory (**Kermani, column 1, lines 10 - 16**) and (**Levenstein, column 1, lines 10 - 17**).

f. The motivation to use the art of Levenstein with the art of Kermani would have been the benefit recited in Levenstein that the invention provides a network

of multiple processing devices in which contentions are resolved rapidly (**column 1, lines 52 - 62**). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Levenstein with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

9. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kermani (U.S. Patent No. 6,314,499) in view of Chrysanthakapoulos (U.S. Patent No. 6,704,819) as applied to claims **1 and 4 - 6** above, and further in view of Schwartz (Schwartz, Mischa; "Telecommunications Networks: Protocols, Modeling and Analysis", 1987, Addison-Wesley).

a. Kermani as modified by Chrysanthakapoulos teaches the multiprocessor array, as recited in claim **1** above.

b. **Regarding claim 7**:

c. Kermani does not specifically teach:

i. A multiprocessor array as claimed in claim 1, wherein said at least one criterion is in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit (17).

d. Schwartz appears to teach:

i. Resource allocation where each resource is statistically allocated a given percentage of the time for accessing the peripheral unit (**page 408, section 8-1-1 Roll-call Polling, first paragraph, especially the sentence that starts with "Stations may be polled more than once during a cycle"; it would have been obvious that this method is functionally equivalent to statistically allocating a given percentage of time for accessing the peripheral unit. Please note that round-robin polling is functionally**

equivalent to statistically allocating an equal percentage of time to each shadow register)(17).

e. The art of Schwartz and the art of Kermani are analogous art because they both contain the problem of shared resource allocation.

f. The motivation to use the art of Schwartz with the art of Kermani would have been the suggestion in Schwartz that polling can be based on priority considerations or respond to variations in traffic (**page 408, section 8-1-1 Roll-call Polling, first paragraph, especially the sentence that starts with "Stations may be polled more than once during a cycle"**).

g. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Schwartz with the art of Kermani and Chrysanthakapoulos to produce the claimed invention.

Conclusion

Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure:

Stirk (U.S. Patent No. 5,408,627)

DeRoo (U.S. Patent No. 6,161,162)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul L. Rodriguez 10/5/05
Primary Examiner
Art Unit 2125